UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,789	03/16/2004	Andy Yu	20359.3	3122

49358 7590 01/12/2006

CARLTON FIELDS, PA
1201 WEST PEACHTREE STREET
3000 ONE ATLANTIC CENTER
ATLANTA, GA 30309

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,789	YU ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26,39 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,22 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *19-21,23,24,26,39 and 40* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/12/2004; 3/18/205; 6/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-26 in the reply filed on December 21,2005 is acknowledged. However, since the Non-elected species have been cancelled, the traversal is moot.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 19-21, 23, 24, 26 and newly submitted claims 39, 40 are directed to an invention that is independent or distinct from the invention originally elected species for the following reasons: inventions memory device claims 1-20, 22 and 25 and method of using the memory device, claims 19-21, 23, 24, 26, 39 and 40 are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case other methods can be used to program, read and erase the same memory device as discloses in Sung (U.S. Patent No. 6,018,178).

Since applicant has elected an invention, memory device, for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-21, 23, 24, 26, 39 and 40 are withdrawn from consideration as being directed to a non-elected invention, method of using. See 37 CFR 1.142(b) and MPEP § 821.03.

Status of the Claims

3. Amendment filed December 21, 2005 has been entered. Non-elected species, claims 27-38 have been cancelled. Claim 7 has been amended. Claims 39 and 40 have been added. Claims 1-26, 39 and 40 are pending. Claims 19-21, 23, 24, 26, 39 and 40 have been further restricted and withdrawn from examining for its merits.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

DUAL FLOATING GATES NON-VOLATILE ELECTRICALLY ALTERABLE MEMORY CELL FOR STORING MULTIPLE DATA.

Claim Objections

6. Claims 6, 10 are objected to because of the following informalities:

Claim 6, recites: wherein the third insulator region having a thickness that allows tunneling of charge between the second floating gate and the first channel region.

The insulator region that allows tunneling of charge between the second floating gate and the first channel region is the second insulator region. (See claim 1, lines 15-18).

Claim 10, recites: wherein the first vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the second floating gate and the control gate, and the first vertical insulator preventing leakage between the second floating gate and the control gate.

The first vertical insulator is between the first floating gate and the control gate. (See claim 1, lines 19-24).

Appropriate correction is required.

7. Claims 18, 22 and 25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for *failing to further limit* the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claims 18, 22 and 25 recite the characteristics of the memory device of claim 1. These terms are the behaviors, read, write or erase, of the memory device of claim 1 upon the application of voltages. Therefore, they do not further limit claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 4, 6, 8, 10, 12, 15, 16, 18, 22 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Sung (U.S. Patent No. 6,018,178).

With respect to claim 1, Sung teaches an electrically alterable memory device as claimed including:

a first semiconductor layer (2) doped with a first dopant (N) in a first concentration;

a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant (P) that has an opposite electrical characteristic than the first dopant, the second semiconductor layer (3) having a top side;

two spaced-apart diffusion regions (14) embedded in the top side of the second semiconductor layer (3), each diffusion region (14) doped with the first dopant (N) in a second concentration greater than the first concentration, the two diffusion regions (14) including a first diffusion region (14aa) and a second diffusion region (14ab), and a first channel region defined between the first diffusion region (14aa) and the second diffusion region (14ab);

a first floating gate (10A) having a first height and comprised of a conductive material, the first floating gate disposed adjacent the first diffusion region (14aa) and above the first channel region and separated therefrom by a first insulator region (9), the first floating gate capable of storing electrical charge;

a second floating gate (10B) having a second height and comprised of a conductive material, the second floating gate disposed adjacent the second diffusion region (14ab) and above the first channel region and separated therefrom by a second insulator region (9), the second floating gate capable of storing electrical charge; and

a control gate (40) having a third height and comprised of a conductive material, the control gate disposed laterally between the first floating gate (10A) and the second floating gate (10B), the control gate separated from the first floating gate (10A) by a first vertical insulator layer (8) and separated from the second floating gate (10B) by a second vertical insulator layer (8), the control gate (40) further being above the first channel region and separated therefrom by a third insulator region (4). (See Fig. 9).

With respect to claim 3, the first dopant of Sung has an N-type characteristic and the second dopant having a P-type characteristic.

With respect to claim 4, the first insulator region (9) of Sung having a thickness that allows tunneling of charge between the first floating gate (10A) and the first channel region.

With respect to claim 6, as best understood by the examiner, the second insulator region (4) of Sung has a thickness that allows tunneling of charge between the second floating gate and the first channel region.

With respect to claim 8, the first vertical insulator (8) of Sung is made from a silicon dioxide having a thickness that provides capacitance between the first floating gate (10A) and the control gate (40), and the first vertical insulator (8) preventing leakage between the first floating gate (10A) and the control gate (40).

With respect to claim 10,as best understood by the examiner, the first vertical insulator (8) of Sung is made from a silicon dioxide having a thickness that provides capacitance between the *first* floating gate (10A) and the control gate (40), and the first vertical insulator (8) preventing leakage between the *first* floating gate (10A) and the control gate (40).

With respect to claim 12, the first height of the first floating gate (10A) of Sung is taller than the third height.

With respect to claim 15, the first floating gate (10A) and the second floating gate (10B) of Sung each being capable of storing multiple levels of charge.

With respect to claim 16, the first floating gate (10A) and the second floating gate (10B) of Sung each being capable of storing four levels of charge.

With respect to claim 18, a charge is inherently transported from the first channel region to the second floating gate (10B) of Sung when a first combination of voltages is applied to the first diffusion region (10aa), the second diffusion region (14ab), the control gate (40), and the second semiconductor layer (3).

With respect to claim 22, charge inside the second floating gate (10B) of Sung can be determined when a second combination of voltages is applied to the first diffusion region (14aa), the second diffusion region (14ab), the control gate (40), and the second semiconductor layer (3).

With respect to claim 25, charge is inherently removed from the second floating gate (10B) when a third combination of voltages is applied to the first diffusion region (14aa), the second diffusion region (14ab), the control gate (40), and the second semiconductor layer (3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178.

With respect to claim 2, Sung teaches the first semiconductor layer is doped with first dopant (N-type) and the second semiconductor layer is doped second dopant (P-type), respectively.

Thus, Sung is shown to teach all the features of the claim with the exception of doping the first and second semiconductor layers with the opposite type dopants.

However, it is well known in the art that dopant N-type or P-type can be used interchangeably to form different characteristics devices, e.g., N channel or P channel devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to dope the first and second semiconductor layers of Sung with any of the opposing dopant type, since it has been held that a mere reversal of the essential working parts, e.g., N-type instead of P-type or vice versa, of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

10. Claims 5, 7, 9, 11, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 as applied to claims 1, 4 and 6 above, and further in view of Hisamune (U.S. Patent No. 5,929480).

With respect to claims 5 and 7, Sung teaches the first and second insulator regions (9) having thickness (60 Å to 70 Å) that allows tunneling of charge between the floating gates (10) and the first channel.

Thus, Sung is shown to teach all the features of the claim with the exception of a thicker insulator region. Note that the thickness range of Sung include the lower end of the claimed range.

However, Hisamune teaches the first and second insulator region (507) can be formed to have thickness of about 100 Å, which is within the claimed range. (See Fig. 9D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulator regions of Sung to a thickness as taught by Hisamune because such thickness still provide tunneling of charge, thus, the scope of Sung teaching is not deviated.

With respect to claims 9 and 11, Sung teaches the first and second vertical insulators (8) are made from a dielectric material having a thickness that provides capacitance between the floating gate (10) and the control gate (40), and the vertical insulators (8) prevents leakage between the floating gates (10) and the control gate (40).

Thus, Sung is shown to teach all the features of the claim with the exception of explicitly using oxide nitride oxide (ONO) for the vertical insulators.

However, Hisamune teaches beside oxide film, a composite film composes of ONO can be used to provides capacitance between the floating gates (508/511) and the control gate (510), and the vertical insulators (512) prevents leakage between the floating gates and the control gate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the vertical insulators of Sung utilizing the composite film ONO as taught by Hisamune since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as matter of obvious design

choice. In re Since it has been held to be within the general skill of a worker in the art to select a known material on the basis of it suitability for the intended use as a matter of obvious design choice. *In re* Leshin, 125 USPQ 416., 125 USPQ 416.

With respect to claim 13, Sung teaches the first floating gate (10A) and the control gate (40) having the first and third heights, respectively.

Thus, Sung is shown to teach all the features of the claim with the exception of the first height being shorter than the third height.

However, Hisamune teaches other configurations of the floating gate and control gate can be used for the dual floating gate memory device including: the first floating gate (508) being shorter than the control gate (510). (See Fig. 9D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the floating gate and the control gate of Sung to the heights as taught by Hisamune since such modification would have involve a mere change in size of the components. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

With respect to claim 17, each diffusion region (504/505) of Hisamune is covered by an oxidation layer (507).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 as applied to claim 1 above, and further in view of Kazerounian (U.S. Patent No. 5,949,711) of record.

Sung teaches the first floating gate (10A) and the control gate (40) having the first and third heights, respectively.

Thus, Sung is shown to teach all the features of the claim with the exception of the first height and the third height being the same.

However, Kazerounian teaches other configurations of the floating gate and control gate can be used for the dual floating gate memory device including: the first floating gate (107) and the control gate (102) has the same height. (See Fig. 7D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the floating gate and the control gate of Sung to the height as taught by Kazerounian since such modification would have involve a mere change in size of the components. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER